CLAIM AMENDMENTS

1. (Currently Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface and a lower surface, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that contacts the lower surface and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, wherein the first housing portion includes a peripheral ledge, and the second housing portion is exposed ~~located~~ within the peripheral ledge ~~and is exposed~~; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

2. (Original) The device of claim 1, wherein the first housing portion contacts four outer side surfaces of the chip.

3. (Original) The device of claim 1, wherein the first housing portion is spaced from the upper surface.

4. (Original) The device of claim 1, wherein the second housing portion contacts the conductive trace.

5. (Original) The device of claim 1, wherein the second housing portion is spaced from the lower surface.

6. (Previously Presented) The device of claim 1, wherein the second housing portion is recessed relative to the peripheral ledge.

7. (Original) The device of claim 1, wherein the first housing portion is a transfer molded material, and the second housing portion is a cured polymeric material.

8. (Original) The device of claim 1, wherein the conductive trace extends through a peripheral side surface of the first housing portion and contacts the second housing portion without extending through a surface of the second housing portion.

9. (Previously Presented) The device of claim 1, wherein the device is devoid of an electrical conductor that extends through opposing surfaces of the second housing portion.

10. (Original) The device of claim 1, wherein the device is devoid of wire bonds, TAB leads and solder joints.

11. (Currently Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that contacts the lower surface and the side surfaces and is spaced from the upper surface and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell and is spaced from the lower surface; and

a conductive trace that extends laterally through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing, wherein the first housing portion spans 360 degrees around the conductive trace at the opening.

12. (Previously Presented) The device of claim 11, wherein the second housing portion includes first and second opposing surfaces, the first surface contacts the light sensitive cell and is spaced from the conductive trace, and the second surface faces away from the chip and is exposed.

13. (Previously Presented) The device of claim 12, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within the peripheral ledge.

14. (Original) The device of claim 13, wherein the second housing portion is recessed relative to the peripheral ledge.

15. (Previously Presented) The device of claim 11, wherein the first housing portion is a transfer molded material, and the second housing portion is a cured polymeric material.

16. (Original) The device of claim 11, wherein the insulative housing consists of the first and second housing portions.

17. (Previously Presented) The device of claim 11, wherein the first housing portion is a transfer molded material that includes a peripheral ledge, and the second housing portion is a cured polymeric material that is located within the peripheral ledge and includes a first surface that contacts the light sensitive cell and is spaced from the conductive trace and a second surface opposite the first surface that faces away from the chip and is exposed.

18. (Original) The device of claim 11, wherein the conductive trace extends through a peripheral side surface of the first housing portion and contacts the second housing portion without extending through a surface of the second housing portion.

19. (Previously Presented) The device of claim 11, wherein the device is devoid of an electrical conductor that extends through opposing surfaces of the second housing portion.

20. (Original) The device of claim 11, wherein the device is devoid of wire bonds, TAB leads and solder joints.

21. (Currently Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and ~~uncurved~~ peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-

piece that contacts the chip, provides the peripheral side surfaces and the bottom surface and is non-transparent, and the second housing portion contacts the upper surface, is farther from the bottom surface than the lower surface is from the bottom surface, does not extend across any of the peripheral side surfaces, provides at least a portion of the top surface, ~~and~~ is transparent and is exposed; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

22. (Original) The device of claim 21, wherein the first housing portion contacts the lower surface and the outer side surfaces and is spaced from the upper surface.

23. (Original) The device of claim 21, wherein the second housing portion contacts the light sensitive cell and the conductive trace and is spaced from the lower surface.

24. (Original) The device of claim 21, wherein the first housing portion includes a peripheral ledge that forms a peripheral portion of the top surface, and the second housing portion is located within and recessed relative to the peripheral ledge.

25. (Previously Presented) The device of claim 21, wherein the first housing portion is a transfer molded material, and the second housing portion is a cured polymeric material.

26. (Original) The device of claim 21, wherein the insulative housing consists of the first and second housing portions.

27. (Previously Presented) The device of claim 21, wherein the light sensitive cell contacts a major surface of the second housing portion that faces towards and is parallel to the upper surface.

28. (Original) The device of claim 21, wherein the device is devoid of an electrical conductor that extends through the top or bottom surfaces.

53. (Original) The device of claim 51, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within and recessed relative to the peripheral ledge.

54. (Original) The device of claim 53, wherein the peripheral ledge includes four inner side surfaces that are opposite the peripheral side surfaces and outside a periphery of the chip.

55. (Original) The device of claim 51, wherein the first housing portion is a transfer molded material, and the second housing portion is a cured polymeric material.

56. (Original) The device of claim 51, wherein the insulative housing consists of the first and second housing portions.

57. (Previously Presented) The device of claim 51, wherein the first housing portion is a transfer molded material that includes a peripheral ledge, and the second housing portion is a polymeric material that is located within the peripheral ledge and includes a first surface that contacts the light sensitive cell and is spaced from the conductive trace and a second surface opposite the first surface that faces away from the chip and is exposed.

58. (Original) The device of claim 51, wherein the device is devoid of an electrical conductor that extends through the top or bottom surfaces.

59. (Previously Presented) The device of claim 51, wherein the device is devoid of an electrical conductor that extends through opposing surfaces of the second housing portion.

60. (Original) The device of claim 51, wherein the device is devoid of wire bonds, TAB leads and solder joints.

61. (Currently Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that contacts the chip, covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that extends laterally through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing, wherein the first housing portion spans 360 degrees around the conductive trace at the opening.

62. (Previously Presented) The device of claim 61, wherein the first housing portion contacts the lower surface and the side surfaces.

63. (Previously Presented) The device of claim 61, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within and recessed relative to the peripheral ledge.

64. (Previously Presented) The device of claim 61, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the opening includes sidewalls that contact and span 360 degrees around the recessed portion.

65. (Previously Presented) The device of claim 61, wherein the device is devoid of wire bonds, TAB leads and solder joints.

66. (Previously Presented) An optoelectronic semiconductor package device, comprising:

76. (Currently Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that includes a lead and a planar metal trace, wherein the lead extends through an opening in the first housing portion, extends outside the insulative housing, does not extend across any edge of the pad and is electrically connected to the pad inside the insulative housing, and the planar metal trace contacts and is not integral with the lead, contacts the first housing portion, extends across one of the side surfaces and does not extend outside the insulative housing.

77. (Previously Presented) The device of claim 76, wherein the first housing portion contacts the lower surface and the side surfaces.

78. (Previously Presented) The device of claim 76, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within and recessed relative to the peripheral ledge.

79. (Previously Presented) The device of claim 76, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one

140. (Previously Presented) The device of claim 136, wherein the device is devoid of wire bonds, TAB leads and solder joints.

141. (Currently Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes first and second insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface, a bottom surface, ~~unecurved~~ peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, and the second housing portion extends into the peripheral ledge, contacts the light sensitive cell, does not extend midway between the upper and lower surfaces outside the chip, does not extend across any of the peripheral side surfaces, ~~and~~ is transparent and is exposed; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

142. (Previously Presented) The device of claim 141, wherein the first housing portion contacts the lower surface and the outer side surfaces.

143. (Previously Presented) The device of claim 141, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

144. (Previously Presented) The device of claim 141, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one

149. (Previously Presented) The device of claim 146, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

150. (Previously Presented) The device of claim 146, wherein the device is devoid of wire bonds, TAB leads and solder joints.

151. (New) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that contacts the lower surface and the side surfaces and is spaced from the upper surface and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is recessed relative to the peripheral ledge; and

a conductive trace that extends through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

152. (New) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that contacts the chip, covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that extends through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the opening includes sidewalls that contact and span 360 degrees around the recessed portion.

153. (New) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that includes a lead and a planar metal trace, wherein the lead extends through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing, the planar metal trace contacts and is not integral with the lead, extends across one of the side surfaces and does not extend outside the insulative housing, and the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that

face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the opening includes sidewalls that contact and span 360 degrees around the recessed portion.

154. (New) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes first and second insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface, a bottom surface, uncurved peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, and the second housing portion extends into the peripheral ledge, contacts the light sensitive cell, does not extend midway between the upper and lower surfaces outside the chip and is transparent; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.